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**DELIVER TO:** Examiner Cao, Phat X Art Unit 2814

**COMPANY:** United States Patent and Trademark Office

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**FROM:** Robert Popa

**DATE:** November 22, 2004

**TOTAL NO. OF PAGES (INCLUDING THIS PAGE):** 9

**SUBJECT :** Response to Second Restriction Requirement  
U.S. Application No. 10/637,848  
Lap-Wai Chow et al.  
"Use of Silicon Block Process Step . . ."  
Our Ref: B-4505NP 620843-6/RPB

**REMARKS:**

Examiner Cao:

Enclosed is a response to the Office Action mailed on October 20, 2004 consisting of:

Response to second restriction requirement - 8 pages

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lap-Wai Chow et  
al.

) Group Art No.: 2814

Application No: 10/637,848

) Examiner: Cao, Phat X

Filed: August 7, 2003

) Re: **RESPONSE TO SECOND  
RESTRICTION REQUIREMENT**

For: "USE OF SILICON  
BLOCK PROCESS STEP TO  
CAMOUFLAGE A FALSE  
TRANSISTOR"

) Our Ref: B-4505NP 620843-6/RPB

) Date: November 22, 2004

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RESPONSE TO SECOND RESTRICTION REQUIREMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

This paper is filed in response to the second restriction requirement set forth in the Office Action dated October 20, 2004, a reply to which is initially due by November 22, 2004 (Monday). Please enter the following amendments and consider the following remarks with respect to the subject application. All amendments and remarks herein are made without prejudice.

Amendments to the claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

\* \* \* \*